ISTC 2025 Implementation Competition

Competition Committee: Henry Pfister, Chair (Duke), Gianluigi Liva (DLR) , Sebastian Cammerer (NVIDIA)

There are a variety of encoding/decoding solutions for short blocklength (e.g. K <= 512 message bits) including (among others) polar codes with CRC-aided successive cancellation list decoding, BCH codes with ordered statistics decoding, polarization adjusted convolutional codes with a variety of decoding approaches, and tail-biting convolutional codes with expurgating linear functions (CRCs) decoded with serial or parallel list decoding. ISTC 2025 will feature a competition to explore the frame error rate, average latency, and maximum latency performance of actual C implementations of short blocklength encoders and decoders running on a single CPU. For this competition, implementation should not use multiple cores or multi-thread coding. Future competitions will address other architectures including GPUs.

The submission deadline is the same as the ISTC paper submission deadline. Each competing organization will submit a conference paper describing the encoder and decoder approach as well as a github library of their encoder and decoder C source code. Both the paper and the source code are treated as confidential information and not disclosed. If accepted, the paper and the performance results of the implementation will be published, but the source code itself will remain confidential unless the author wishes to release the source code so that others can replicate their amazing performance.

There are a variety of categories for the competition. To submit a paper to the competition you should plan to submit C source code for an encoder/decode repair for at least one column (all three rates for a given K) or one row (all four values of K for a given rate) of the configurations listed below. We encourage submission of encoder/decoder pairs that operate for all twelve configurations as would be required in a standard. For each rate, we will simulate your code to measure FER performance and latency with particular attention to performance near the FER operating points of 10^-3 and 10^-6. Your source code will need to include certain lines that allow us to measure latency (instructions to follow).

Rate	$K = 64$ message bits	$K = 128$	$K = 256$	$K = 512$
$R = 1/4$	$(N = 256, K = 64)$	(512,128)	(1024,256)	(2048,512)
$R = 1/2$	(128,64)	(256,128)	(512,256)	(1024,512)
$R = 4/5$	(80,64)	(160,128)	(320,256)	(640,512)

The FER and latency performance of all submissions will be presented in a talk at the conference and a team of judges will determine winning encoder/decoder pairs for each row and each column as well as an overall winner.